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Status of the CMS Pixel detector

D. Kotliński^{1,2}

*Paul Scherrer Institut,
CH-5232 Villigen, Switzerland*

E-mail: danek.kotlinski@psi.ch

ABSTRACT: After 10 years of design and construction the CMS pixel detector has been installed and commissioned. The pixel detector which has two parts, barrel layers and forward disks, consists of 66 M pixels of $100\ \mu\text{m} \times 150\ \mu\text{m}$ size. In the paper the detector installation, commissioning and the results of the detector testing is presented. The basic electronic parameters of the detector like noise, threshold and the analog signal calibration are shown. The detector performance is illustrated by showing the pixel response uniformity and the number of dead channels.

KEYWORDS: Particle tracking detectors; Solid state detectors; Large detector systems for particle and astroparticle physics

¹Corresponding author.

²for the CMS Pixel Collaboration

Contents

1	Introduction	1
2	Detector installation	2
2.1	Final construction and integration	2
2.2	Pixel infrastructure in P5	3
2.3	Installation	4
3	Testing and calibration	6
3.1	Sequence of tests and calibrations	6
3.2	Baseline and address level calibrations	7
3.3	Clock and delay adjustments	9
3.4	Threshold and noise measurements	10
3.5	Analog signal response calibration	11
4	Detector performance	11
4.1	Overview	11
4.2	Dead modules, dead and noisy pixels	11
4.3	Noise	12
4.4	Threshold	13
4.5	Gain calibration	15
4.6	Charge collection	16
5	Conclusions	17

1 Introduction

The CMS pixel detector consists of a central barrel and pairs of forward disks. The three 53 cm long barrel layers are located at mean radii of 4.3 cm, 7.2 cm and 11.0 cm. The two pairs of forward disks are placed 34.5 cm and 46.5 cm from the barrel center. In order to achieve the optimal vertex position resolution in both the ($r\phi$) and the z coordinates a design with an almost square pixel shape was adopted. To enhance the spatial resolution by analog signal interpolation the effect of charge sharing induced by the large Lorentz drift in the 4T magnetic field is used. Hence the detectors are deliberately not tilted in the barrel layers but are tilted in the forward disks resulting in a turbine like geometry. The use of signal interpolation means that full analog information has to be transferred from each hit pixel. More detailed discussion of the detector layout and geometry can be found in [1, 2]. An introduction to early hybrid pixel detectors can be found in [3]. Second generation hybrid pixel detectors, like the one described here, have also been built for other LHC experiments: ATLAS [4] and ALICE [5].

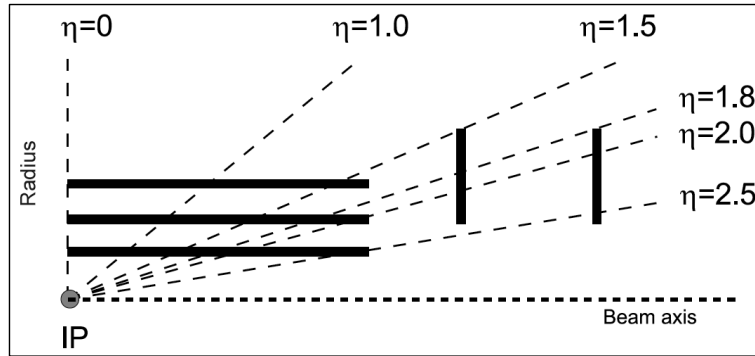


Figure 1. Rapidity coverage of the CMS pixel detector

A very schematic geometrical layout of the CMS pixel detector is shown in figure 1. The barrel (BPIX) consists of 768 detector modules arranged into half-ladders of 4 identical modules each. The forward disks (FPIX) consist of 672 detector modules of 7 different sizes arranged into blades. A photograph of the fully assembled pixel barrel detector is shown in figure 2 and the forward detector in figure 3.

To read out the detector about 16000 readout chips (ROCs) are bump-bonded to the detector modules. The pixel size is $100 \times 150 \mu\text{m}^2$, with the shorter, $100 \mu\text{m}$ side, in the $r\phi$ direction for the barrel and the r direction for the endcaps. More details about the readout chip can be found in [6]. The silicon pixel sensors are described in [7] for the barrel and in [8] for the forward pixels.

In the CMS electronics room two types of VME modules, the front-end driver (FED) and the front-end controller (FEC), are used. The FED is a readout module, it digitizes the analog input signals, builds event fragments and sends them to the DAQ. The FEC is responsible for sending the clock, trigger and other signals to the front-ends. The connection between the front-ends and the FEC/FED is provided by optical links, analog for the readout part and digital for the control part. The read out and control has been described in details in [9].

More details about various aspects of the CMS pixel detector are given in other contributions to these proceedings. The commissioning of BPIX is reviewed in [10] and the FPIX in [11]. The detector control, safety and readout systems are described in [12]. In [13] the plans for the detector upgrade are presented.

2 Detector installation

2.1 Final construction and integration

The pixel barrel detector was fully assembled at the Paul Scherrer Institute (PSI) in Switzerland. The module production, which was done at PSI, took about 2 years and was finished in April 2008. This included the in-house bump-bonding of the readout chips to the sensors, for more details about the module construction and testing see [10]. The mounting of the modules on the barrel mechanical structure and the integration with the supply tubes took place between January and May 2008 (see [10]). Only two months, May and June, were available for the BPIX testing and commissioning at PSI. A photograph of the fully assembled pixel barrel detector is shown in

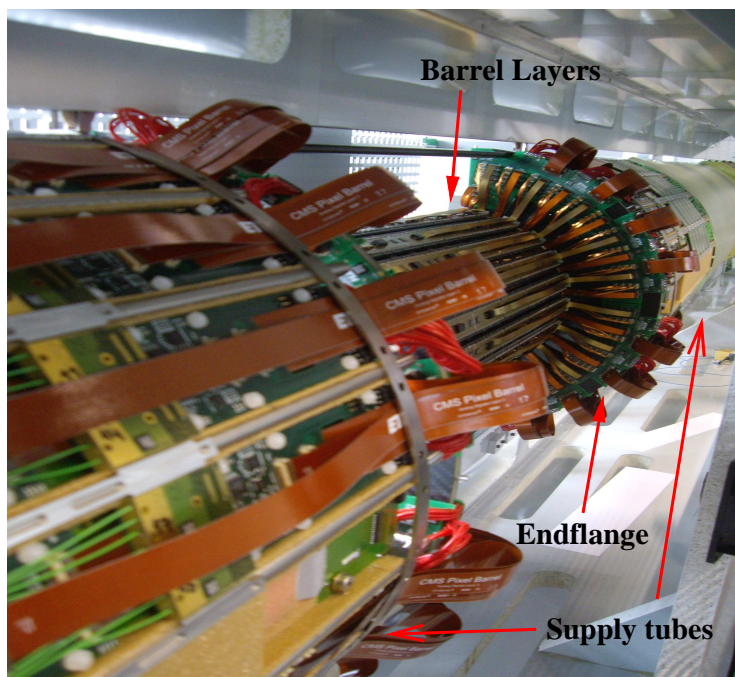


Figure 2. Half of the fully assembled barrel pixel detector in its transport box.

figure 2 where the barrel layers together with the 2 supply tubes are placed inside the transport box. In the middle of July the whole BPIX detector was transported to LHC/P5 in Cessy where the CMS experiment is located. After the transport a quick test of the main detector functionality was performed in order to check if there were any faulty connections, broken cables, bad contacts etc. No new, transport induced, problems were found.

The forward pixels were build at the Fermi National Laboratory (FNAL) in USA. The FPIX modules (called panels) were produced between mid 2006 and the end of 2007. They were assembled on blades and forward disks in 2007 and shipped to CERN in 4 separate pieces. Each of the four pieces was fully tested and commissioned at the TIF (CMS tracker integration facility) in CERN from January to July 2008, for details see [11]. A photograph of the fully assembled forward detector can be seen in figure 3, where the one-half shell of the forward disk together with its supply tube is shown. The FPIX detector was transported to LHC/P5 in mid July 2008.

2.2 Pixel infrastructure in P5

The detector infrastructure in P5 had to be ready well in advanced of the detector installation. This included the installation and commissioning of the power supply system (from CAEN) and the detector safety system (from Siemens). Both are described in more detail in [12]. One of the problems encountered was that the power supply modules were arriving late (due to production delays) and could not be fully tested before installation in the underground cavern.

The cables and fibers between the electronic racks and the detector were placed in winter and spring of 2008. All cables and fibers were tested, these included connectivity tests as well as measurements of the quality of signal transmission.

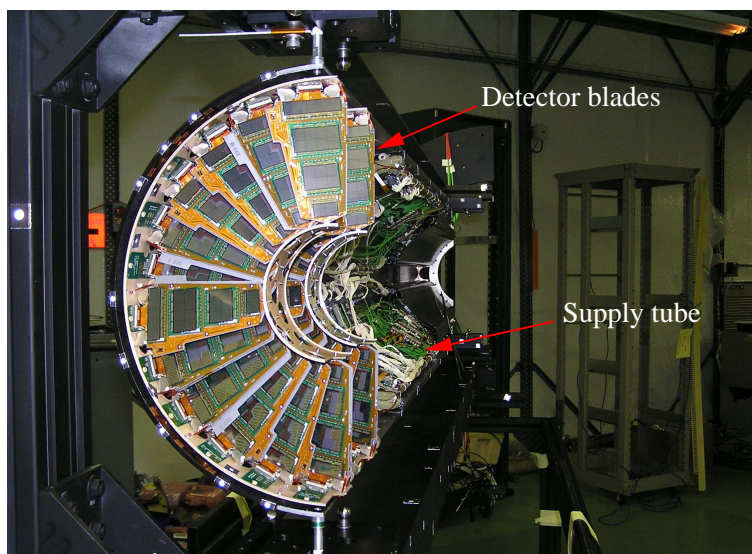


Figure 3. Half shell of the forward pixel detector.

The VME readout cards (FEDs) and the VME control cards (FECs) were installed and tested already at the end of 2007. Some tests were done with the CMS-DAQ using emulation mode (sending fake signals). A small scale pixel detector (called “pixel-in-box”) was mounted in the experimental cavern. This was used to test the principle concept of the operation of all aspects of the pixel detector like powering, control, programming and readout.

The pixel detector consumes about 3.6 kW of power. Liquid phase cooling with C_6F_{14} is used to run the detector at temperatures from room temperature down to -10°C [1]. The design and construction of the Pixel cooling plant was overseen by CERN. After installation the cooling system still needed a few months of testing and commissioning by a team of CERN, CMS tracker and pixel experts. Several components of the cooling system had to be repaired or modified. Most of the major issues, including coolant leaks, were resolved before the detector was connected.

2.3 Installation

The pixel detector was the last sub-detector to be installed inside CMS. The detector and its supply tubes fit between the strip tracker volume which starts at a radius of about 21 cm and the beam pipe which has a radius of 2.9 cm. The beam pipe close to the interaction region does not have a constant diameter, there is a conical section within the pixel volume.

The barrel pixel detector was lowered to the underground CMS cavern on July 23rd. It was moved in two independent parts, the inner (+x in the CMS coordinate system) and the outer (-x) shells. Each shell consisted of the detector itself and the two supply tubes at -z and +z. The whole assembly was about 5 m long, 18 cm high and 20 cm wide. After installation of the special rail system the +x detector was rolled into the space available between the strip tracker and the beam pipe. The next day the second, -x, shell was inserted and the cabling process could be started. In figure 4 a photograph of the BPIX detector during the installation of the -x (outer) shell is shown, the barrel layers and the service tubes are visible. The +x (inner) shell is already installed and only its cables and fibers can be seen.

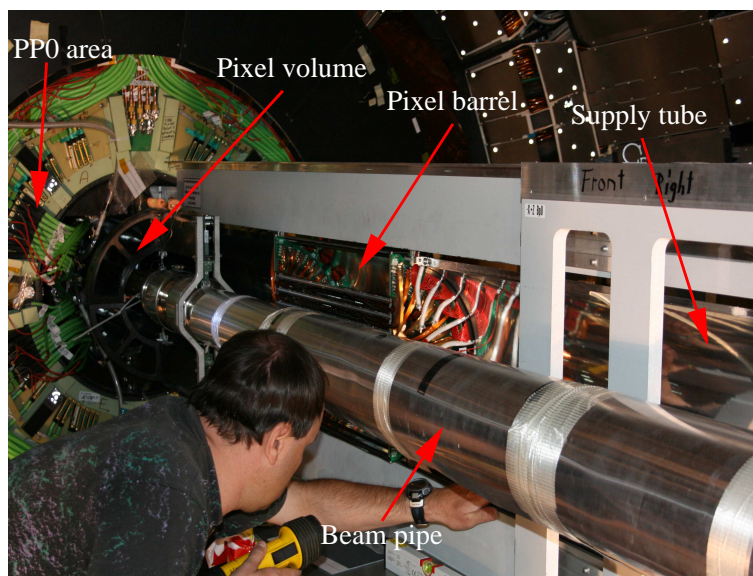


Figure 4. Installation of the second BPIX shell (-x).

The detector is connected to its services in the so called PP0 area, mounted at the end of the strip tracker. First the 20 BPIX cooling tubes were connected using stainless steel below pipes. Then the 80 power and control cables were connected, finally the 36 multi-fiber connections were made. After starting the cooling flow the detector was powered and the first preliminary tests of the basic detector functionality started. Only a few copper cables had to be reconnected but many optical signals were found to be faulty due to dirty optical connections. The connectors had to be cleaned, in some cases many times, before a good connection was established.

On July 29th the BPIX detector worked sufficiently well to give green light for the installation of the forward pixel detector. The FPIX detector was lowered into the cavern in 4 parts, +z and -z and +x (inner) and -x (outer) half shells. First the two shells on the -z side were installed and connected, the next day the two +z shells followed. The photograph in figure 5 shows the insertion of the first +x FPIX shell. The two forward disks are visible and the inside of the supply tube can be seen. It can also be seen that the BPIX cables and fibers had to be disconnected for the FPIX insertion. All FPIX services were connected on July 31st, this included 16 cooling tubes, 60 cables and 16 multi-fiber connectors.

Finally the testing of the whole pixel detector could start. In the first step only the most basic functionality tests were done in order to check the correctness of all connections. This included the testing of:

- clock and trigger distribution,
- front end programmability,
- quality of the readout signals,
- bias connections.

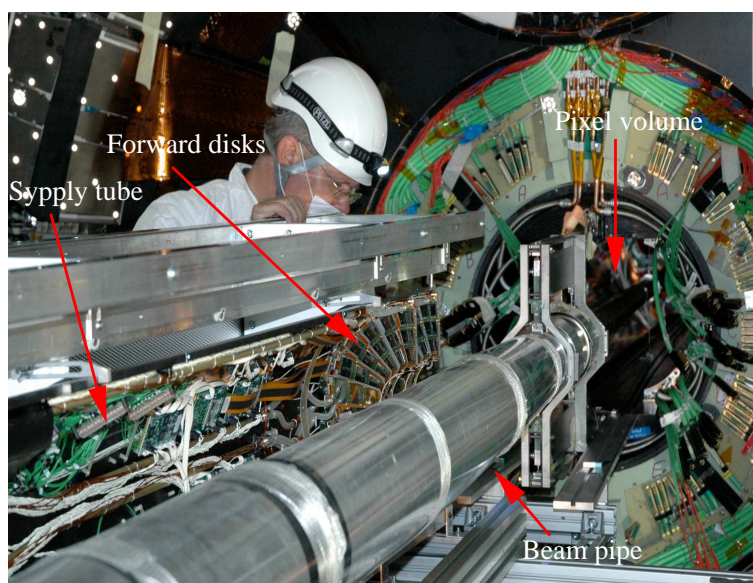


Figure 5. Installation of the 1st FPIX half shell on the -z side.

This was successfully accomplished a few days later. On August 7th all access to the pixel detector was lost due to a very tight schedule of the CMS detector closing.

3 Testing and calibration

3.1 Sequence of tests and calibrations

The fast detector tests, as described in section 2.3, were mostly done with simple standalone software. The final testing and calibration was done using the CMS on-line framework XDAQ [15]. This framework is based on supervisor processes running in a distributed system and communicating through the SOAP protocol, web based GUIs are used for control. For the pixel detector testing and calibration a local pixel DAQ is used which is independent from the high speed CMS DAQ. This means that all the data is read out through VME directly to the control PCs and not through the fast DAQ links (so called S-Links). This has the advantage of being completely independent from the central DAQ services but has a big disadvantage of a relatively low readout speed. Reading data from 16 pixel FEDs through a single VME to PC interface limits the rate to at most 10 events per second. There are plans to use the central DAQ for the more time consuming calibrations (e.g. the gain calibration) but they have not yet been fully implemented.

Most of the calibrations produce directly the resulting new settings which can then be used in subsequent runs. Other calibrations write binary data files which have to be analyzed offline, these include the pixel alive test, the threshold and noise measurement (called “S-curve”) and the gain calibration.

The sequence of the calibrations needed to operate the pixel detector is the following:

1. Adjust the relative delay of the clock to the programming data to make sure that the start and stop conditions are recognized for the 40 MHz modified I2C protocol which is used to

program the front end ROCs and TBMs. It was sufficient to do this adjustment only once at the beginning of test period (more detail in section 3.3).

2. Tune the laser bias in the AOH to produce a sufficient signal. This is done by increasing the bias current until the separation between the analog “black” and “ultra-black” (our two reference signals, see [6]) saturates. This calibration had to be redone each time the detector operating temperature had changed.
3. Adjust the clock phase of the ADCs in the FEDs (more detail in section 3.3). It has to be adjusted each time the phase of the clock is changed, e.g. after the tuning of the fine clock delay.
4. Program the “ultra-black” signals of the ROCs and TBMs to the correct amplitude [6]. Has to be repeated each time item 2 changes.
5. Adjust the baseline of the analog signal arriving to the ADC to be in the middle of the range. This is done by tuning individual offsets which are included in each input channel of the FED. This procedure has to be performed very often, for more details see section 3.2.
6. Select a threshold and delay setting for each ROC in such a way that the injected test charge (called VCAL signal) is correctly registered and readout. Adjusted only once at the commissioning start.
7. Run the address level calibration. Repeated often, more details in section 3.2.
8. Run the pixel alive test. This is the basic test which shows if pixels function correctly and respond to the VCAL injection. It does not verify anything related to the sensors, that is it neither checks that the bump-bonds are OK nor that the bias HV is on.
9. Run the “S-curve” test to measure the pixel thresholds and noise. This is only done after the threshold adjustment or if some basic operational parameter changes e.g. the detector temperature. It is discussed more in section 3.4.
10. Run the gain calibration to measure the pixel analog response. Needs to be done seldom, only when a basic detector parameter like the temperature or the LV power is modified. In practice it was performed about once a month. It is discussed more in section 3.5.

In the next subsections some of these calibrations will be discussed in more detail.

3.2 Baseline and address level calibrations

As mentioned before the detector uses analog readout which means that the signal stability is very important. Unfortunately the AOH (analog optical hybrid [9]), which is used to convert the electrical analog signal to optical, is very temperature sensitive. Already 1 degree temperature change shifts the signal by 50 ADC counts (out of 1024). The pixel FED automatically corrects for baseline shifts during a run but it is important to start with a uniform baseline distribution. The baseline calibration adjusts each optical input to be ± 5 counts from a preselected value (usually 450). This calibration cannot be run during data taking so if the baseline drift is too large for the automatic correction to work correctly the data taking has to be stopped. Present experience, from

the cosmic run in 2008, shows that if the temperatures are stable within 1 degree the automatic baseline corrections works correctly. Data were acquired for periods of up to 48 hours without the need to recalibrate the baseline corrections. In periods when the silicon strip detector went through power cycles the temperature variations were larger than 1 degree and the pixel detector had to be dropped from the CMS DAQ and re-calibrated. This calibration is relatively simple and fast, therefore after about 5 minutes the detector was again ready for data taking. In the normal LHC operations it is planned to perform the baseline calibration at least once a day during the LHC fills.

As explained in many references (e.g. [6]), the pixel ROC uses analog signals to also transmit digital information, e.g. the pixel addresses. The main reason for this choice is the following:

- The 4 T magnetic field produces a relatively large Lorentz drift angle (26°) and generates a substantial charge sharing between pixels. In order to take advantage of this effect the pixel charge has to be recorded.
- At the time of the detector design it was decided that implementing a 6 bit ADC in each ROC was not possible due to space and power limitations. Thus, the pixel charge has to be transmitted as an analog signal to the readout electronics. The analog signal transmission cannot be done at a too high speed therefore, a 40MHz analog fiber link was selected.
- The same link has to be used to transmit the digital information e.g. the pixel address. Transmitting digital information at 40MHz rate is slow and would require a significantly larger number of optical links. Therefore, it was decided to encode the digital information into an analog signal using a 6 level coding and reducing the number of the needed clock cycles by a factor of 2.5.

After the signal transmission and digitization the correct addresses have to be decoded in the FEDs. The correctness of this process depends on the good calibration of the address levels and on the long term stability. The stability is related to the baseline correction as discussed in the previous paragraph. The address level calibration has to be done before data taking and the resulting parameters have to be downloaded to each FED. An example of the address level calibration is shown in figure 6, where six peaks, corresponding to the 6 address levels can be seen. The separation between the levels is good. The smallest distance between 2 peaks is 78 ADC counts which with the average RMS of 3.0 gives a relative separation of 26. A few signals are affected by dirty optical connectors and poor light transmission, for such channels the relative separation can be as low as 10, however this is still sufficient to reconstruct the address correctly. The quality of the address level separation is monitored during the run by watching for:

- Invalid pixel address values.
- Incorrect event numbers coming from the TBM chips which are also transmitted using analog encoding.
- Uniformity of the pixel address distributions.

Problems were only encountered when there were large temperature changes and the automatic baseline correction was exceeding 150 ADC counts. For stable running conditions it was sufficient

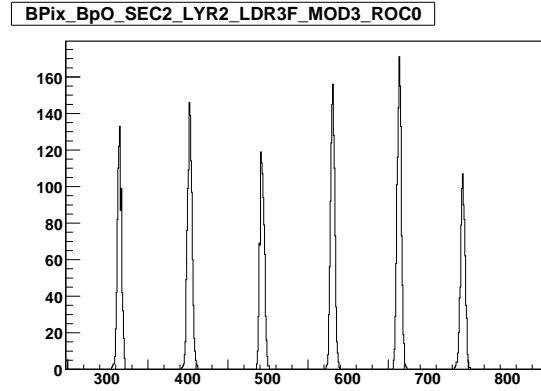


Figure 6. An example of the address level separation in one of the pixel ROCs

to repeat the address level calibration once every few days. During LHC operations this will be done before each LHC fill. The present experience shows that the analog signal readout is reliable and should improve the position resolution due to weighted interpolation between pixels. However, it does require good signal calibration and careful data quality monitoring.

3.3 Clock and delay adjustments

Several time/clock related parameters have to be adjusted for the pixel detector to work correctly. As mentioned earlier the front end ROCs and TBMs are programmed using a 40 MHz modified version of the I2C protocol. This protocol requires a precise phase adjustment between the clock and the data lines in order to recognize the start and stop conditions of the data packets. The plateau of the correct phase is about 6-8 nanoseconds wide and can be different for different parts of the detector. The delay is adjusted by programming the DELAY25 chip [9] which is included in each of the 96 control networks. The phases were adjusted for all control networks at the beginning of the detector commissioning and were then used without any recalibration for the rest of the 3 months long cosmic running period.

The quality of the analog signal can deteriorate due to the non-optimal phase adjustment of the ADC clock in the pixel FEDs. For each of the 1300 incoming analog channels this phase was optimized for the best signal resolution. It was sufficient to adjust these phases only once at the beginning of the detector commissioning. Later it was modified only once, due to the modification of the fine phase of the global clock.

The pixel ROC performs data sparcification and allows the readout of only triggered data. In order to read the correct data the trigger delay has to be known and should be programmed into the so called WBC register of each ROC. The trigger delay, that is the value of the WBC registers, has been estimated from the known cable/fiber lengths and electronic delays. The initial value of 153 (which represents the data to trigger delay in LHC clock units) did not work correctly but shifting it down to 152 was enough to synchronize the trigger with the pixel detector.

After the main detector synchronization there is still the fine phase of the clock (from 0 to 25 nanoseconds) which needs to be optimized. This phase determines the efficiency for registering small amplitude signals for which the time-walk of the front-end amplifiers shifts the timing. The

delay is adjusted by using the same DELAY25 chip as mentioned above. It is impossible to adjust this delay precisely with the very low intensity cosmic rays, the final adjustment has to be done with the LHC beam. However a very coarse scan was performed and some improvement in the rate of the registered cosmic hits was achieved during the CMS cosmic run.

3.4 Threshold and noise measurements

The detection thresholds are an important parameter of the pixel detector since they influence the hit position resolution. Adjusting the thresholds is called trimming and involves optimizing a global threshold parameter for each ROC and adjusting a 4 bit DAC in each pixel cell. The second step is needed in order to make the pixel thresholds uniform. The trimming procedure is based on measurements of the thresholds for a wide range of parameters and then, through interpolation, setting them to a preselected value. With the number of pixels being very large (66M) this procedure is complex and very time consuming. A successful trimming procedure was developed during module testing [10] but it is too slow and requires too much interactivity to be applied for the whole detector in P5. Subsequently a simplified procedure has been implemented in our on-line software.

The thresholds are measured through the so called “S-curve” scan where for each pixel the amplitude of the injected test charge (VCAL) is varied from 0 to its maximum. The VCAL value where the signal shows 50% efficiency is defined as the threshold.

Due to the finite rise-time of the signals the threshold measurement is somewhat more complicated. One should distinguish the absolute threshold defined as the comparator level above which the signal is accepted and the pixel hit is available for readout, and the “in-time” threshold where the signal is fast enough to be correctly labeled by the right bunch crossing. The difference between the two is due to time-walk and is related to the speed of the pixel amplifier. The “absolute” threshold is relevant when discussing noise and cross-talk, that is the optimum conditions under which the ROC still works. It also determines the pixel detector hit occupancy. The “in-time” threshold determines the lowest amplitude signals useful for hit reconstruction and affects the position resolution. Both thresholds can be measured using the “S-curve” method, in the “in-time” measurement the WBC (trigger delay) is set to the nominal value which is presently 152. For the “absolute” threshold measurement the WBC is set to 151 making the readout of the lowest amplitude (i.e. slowest) signals possible.

As a byproduct of this method the noise can also be measured since it is proportional to the width of the region where the signal efficiency switches from 0 to 100%. Both quantities are measured in VCAL units, that is as a function of the parameter which determines the magnitude of the injected charge. The calibration of the VCAL unit itself varies from pixel to pixel and from ROC to ROC. On the average one VCAL unit corresponds to 65.5 electrons, this parameter is referred to as the slope, the average offset is -414 electrons. However, the spreads of the two distributions are rather large, the slope parameter has an RMS of 9 and the RMS of the offset is about 570.

Running the S-curve analysis for the whole detector would take, with the present version of our software, very long. Instead, for each ROC the thresholds are measured using only 81 pixels. Additional tests, performed on part of the detector, where all pixel were used, showed that using 81 pixels is sufficient to determine the average threshold and noise for each ROC. The results of the noise and threshold measurements are shown in sections 4.3 and 4.4.

3.5 Analog signal response calibration

The analog signal has to be calibrated in order to correct for differences in the readout chain. The signal is calibrated versus the injected VCAL signal. For each pixel about 30 charge values are injected. From the response curve each pixel can be calibrated and the obtained calibration constants are used in the data reconstruction. To sample the non-linear part of the response the charge is scanned in non-equidistant steps. During the scan (called gain calibration) the acquired data is stored in binary files and is later analyzed offline. All pixels have to be calibrated therefore the procedure is long and takes about 8 hours for the whole detector. The results of the gain calibration are shown in section 4.5.

4 Detector performance

4.1 Overview

The results presented below are based on a 2 week calibration period in August 2008 and an almost 3 month long global CMS run which lasted until mid November 2008. The global run had a period with the early LHC beam, however the pixel detector was then switched off for safety reasons. The rest of the time was divided into cosmic runs with and without the 3.8 T magnetic field, and shorter, few day, periods for additional detector adjustments and calibrations

Initially the detector was run at about room temperature with the coolant at 17°C, the temperature difference between the coolant and the active detector parts has been estimated to be about 6°C. In the middle of the running period the coolant temperature was lowered to 10°C. All data taken during the longer run with the magnetic field (called CRAFT in CMS) was with the lower detector temperature.

The operation of the pixel detector was interrupted about once a week due to the cooling plant problems. About once a month a power supply failure occurred and the faulty unit had to be replaced. In both cases the interruption lasted for a few hours. Together with some regular failures of the detector control PVSS based software [12] this resulted in an overall efficiency of the data taking being about 97%. The detector was also switched off, for safety reasons, during the magnet “fast” dumps when the magnetic field is lowered very fast.

4.2 Dead modules, dead and noisy pixels

Before detector installation the FPIX part of the detector was in a perfect state, all modules worked correctly. After the installation the detector developed a short on the digital power in one detector segment (135 ROCs). In addition 101 ROCs developed HV problems and 24 ROCs had a very low signal (probably due to a broken wire bond). All together these failures represent 6% of the FPIX detector, therefore for most of the cosmic run the FPIX detector efficiency was 94%. During the winter shutdown 2008-2009 it is planned to repair and reinstall the FPIX detector.

The BPIX detector had some problems already after assembly. Several attempts were made to fix the problems by exchanging modules, however each intervention produced new failures and it was decided to leave the detector with the following bad modules:

- No high voltage connection, 1 module, 8 ROCs.
- Broken signal wire-bonds, 3 modules, 32 ROCs.

Table 1. Pixel noise in electrons, see text for the explanation of the labels.

	Mean	RMS	ROC-RMS
FPIX	85	26	22
BPIX	141	35	27

No additional problems were found after the transportation, however after the detector installation into CMS several more broken modules appeared:

- No high voltage connection, 3 modules, 32 ROCs.
- Broken signal wire-bonds, 1 module, 8 ROCs.
- Cannot be programmed, 1 module, 16 ROCs.

In addition single, randomly placed, 4 ROCs did not give a signal and were disabled. All together this corresponds to 100 non performing ROCs, which represents 0.87% of the BPIX detector. All these failures appeared rather soon after the installation and no new problems were later observed during the whole cosmic run. Presently it is not planned to remove the BPIX detector during the winter shutdown.

The number of dead pixel cells is very small. The ROCs tend either to work very well or not at all. For the BPIX there are about 0.010% dead pixels, for the FPIX this number is also very low, below 0.015%. The number of faulty bump bonds, which also makes a pixel cell useless, could not be measured with the low cosmic track rate. From the module testing this number is known to be about 0.01% [10], therefore all together we expect a total dead pixel rate from permanently damaged pixel to be only 2×10^{-4} . This is a very small number, much smaller than the expected dynamical pixel losses. These losses, due to high data rates, at the full LHC luminosity are expected to be up to a few percent [1, 14] and will therefore dominate the missing pixel rate.

A number of pixels had to be masked off (disabled) due to their high noise. With the “noise” threshold set to 0.001 (this threshold is defined as the ratio of events with the pixel on to all events) the number of masked pixels is 263 for the BPIX and 17 for the FPIX. Within the BPIX noisy pixels there are 2 full ROC rows and one full ROC column, the rest are spread randomly. With a lower threshold of 0.0001 there are 8 more noisy BPIX, and 5 more noisy FPIX pixels, these have not been masked yet. The total fraction of noisy pixels is very low, below 0.5×10^{-5} .

4.3 Noise

As explained in section 3.4 the pixel noise has been measured through the “S-curve” scan. The measured noise is summarized in table 1 in electron equivalent units. The “Mean” is the average noise for all pixels, “RMS” is the RMS of the distribution of all measured pixels, “ROC-RMS” is the mean RMS of the noise variation within single ROCs. The fact that the value of RMS is similar to ROC-RMS means that noise variation is random. That is the noise level is roughly similar for all ROCs and is dominated by the pixel-to-pixel variation.

The average noise of the FPIX detector is significantly lower than the BPIX. The origin of this effect is not completely understood. It can be partly explained by the different design of the sensors

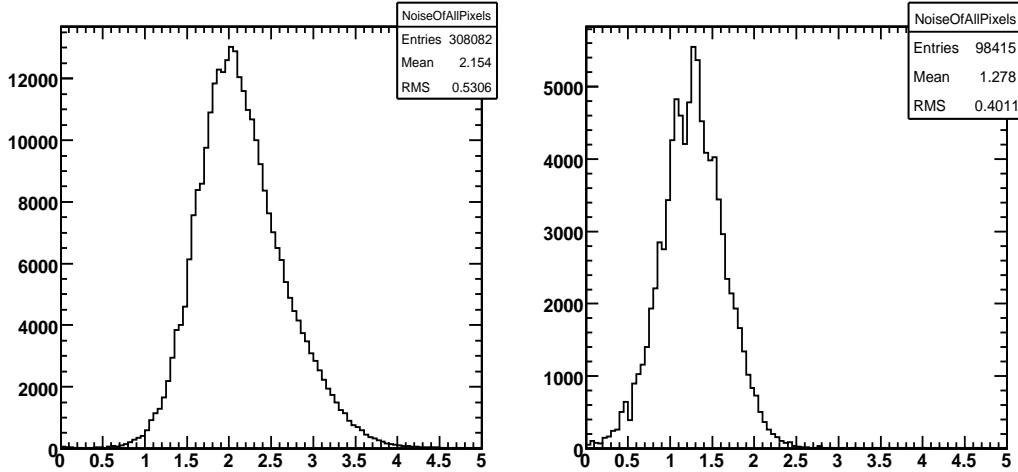


Figure 7. Noise distribution for the BPIX (on the left) and the FPIX (on the right) detectors in units of VCAL (1 VCAL = 65.5 electrons).

which results in a different pixel capacitance. The measured noise is somewhat lower than the one observed during the module testing where it was 110 electrons for the FPIX [11] and 155 for the BPIX [10]. The noise distributions in VCAL units are presented for the BPIX and FPIX detectors in figure 7.

At this very low level the noise has no negative influence on the operation of the detector. The pixel thresholds depend much more on the signal cross-talk than on the noise. It should be stressed that what is measured here is the internal noise inside the pixel cell. The analog signal, as measured by the ADC in the FED, has a much larger noise with multiple contributions from the signal amplifiers, lasers and other optical components. The full readout chain adds noise which is equivalent to 300 electrons [1].

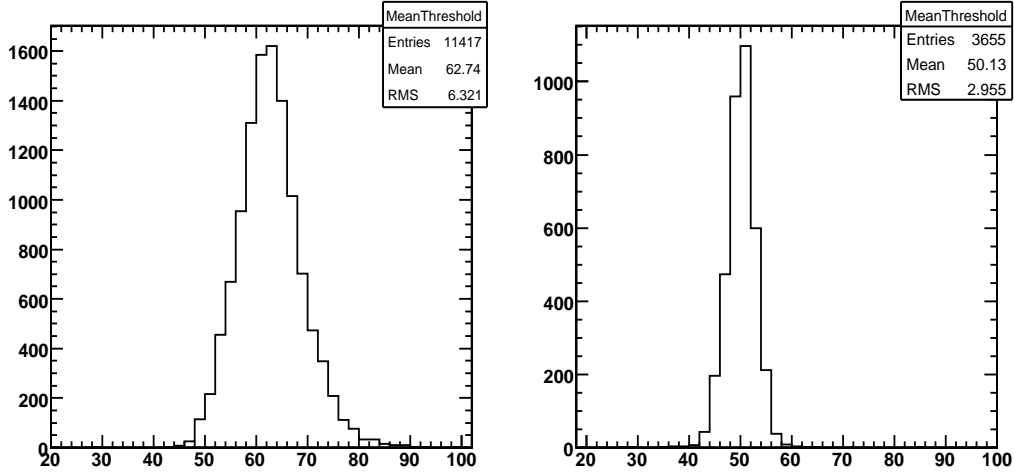
4.4 Threshold

There were some differences in the threshold adjustment between the BPIX and FPIX detectors. Having fewer channels it was possible to adjust the FPIX thresholds to a well defined value before the CMS cosmic run started. For the BPIX part a different strategy was adopted, the trim bits which were determined during the module testing were used and only the global ROC threshold registers were adjusted. It has been shown before that the trim bits are relatively independent of the other parameters and therefore do not have to be readjusted. Initially, due to the lack of time, the global ROC thresholds were only approximately tuned using a simple pre-calibration method. A more complete threshold adjustment could only be done after the cosmic run was finished in November 2008.

Table 2 summarizes the threshold measurements, the results are give in units of electrons. For the BPIX two rows are shown, the one labeled “BPIX” corresponds to the conditions with which the cosmic-ray data were taken, the one labeled “BPIX-new” shows the optimized values obtained later, after the cosmic run was finished. In the table “Mean” is the average pixel threshold, “RMS” is the RMS of the ROC average threshold distribution and “ROC-RMS” shows the average RMS

Table 2. Pixel thresholds in electrons, see text for a more detailed explanation of the labels.

	Mean	RMS	ROC-RMS
FPIX	2870	200	220
BPIX	3690	410	88
BPIX-new	2910	80	80

**Figure 8.** Average ROC threshold distributions for the BPIX (on the left) and the FPIX (on the right) detectors in units of VCAL (1 VCAL = 65.5 electrons).

of the threshold distribution within single ROCs. The value of “RMS” shows how well the ROCs are tuned with respect to each other using the ROC global threshold register. The value of “ROC-RMS” shows the quality of the trimming mechanism which equalizes pixel thresholds within a single ROC.

For both BPIX and FPIX a low threshold of about 2900 electrons was achieved. The quality of the pixel trimming (ROC-RMS) is somewhat better for the BPIX, however in both cases the threshold spread is small enough not to degrade the detector performance.

The average threshold distributions for all ROCs, as used during the recent cosmic run, are presented for the BPIX and FPIX detectors in figure 8. The ROC-RMS of the threshold distributions are show in figure 9.

As explained in section 3.4 both, the absolute and the in-time thresholds have to be considered. In table 3 the absolute thresholds are compared with the in-time thresholds. The average difference between the two is larger for the BPIX, around 1000 electrons, than for FPIX, where it about 600 electrons. This is still not completely understood but probably has to do with the difference in the amount of power delivered to the pixel amplifiers which can influence the time-walk. For the next year it is planned to lower the threshold to 3000 electrons and to equalize the BPIX and FPIX detectors.

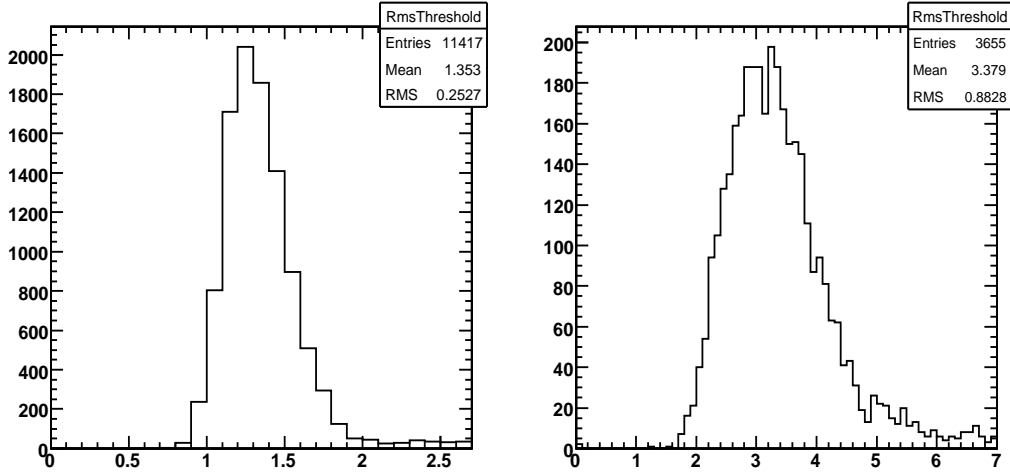


Figure 9. The RMS of the threshold distributions within single ROCs for the BPIX (on the left) and the FPIX (on the right) detectors in units of VCAL (1 VCAL = 65.5 electrons).

Table 3. Absolute and in-time thresholds in electrons.

	Absolute Mean	Threshold RMS	In-time Mean	Threshold RMS	Difference Mean
FPIX	2870	200	3500	150	630
BPIX	3690	410	4730	410	1040
BPIX-new	2910	80	3860	140	950

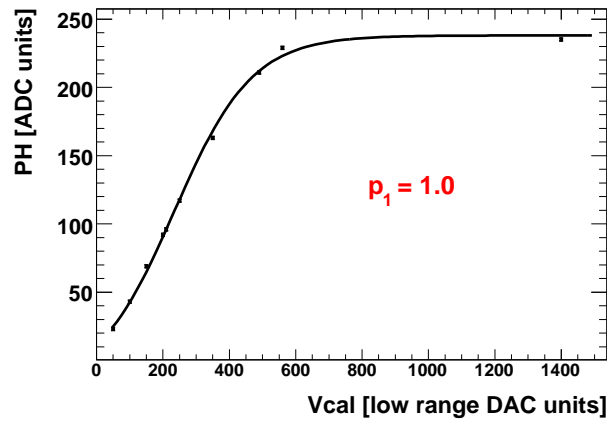


Figure 10. Signal response function for a single pixel.

4.5 Gain calibration

A typical analog signal response of the pixel readout chain is shown in figure 10 where the pulse height measured in the ADC is plotted versus the pixel injected charge (VCAL).

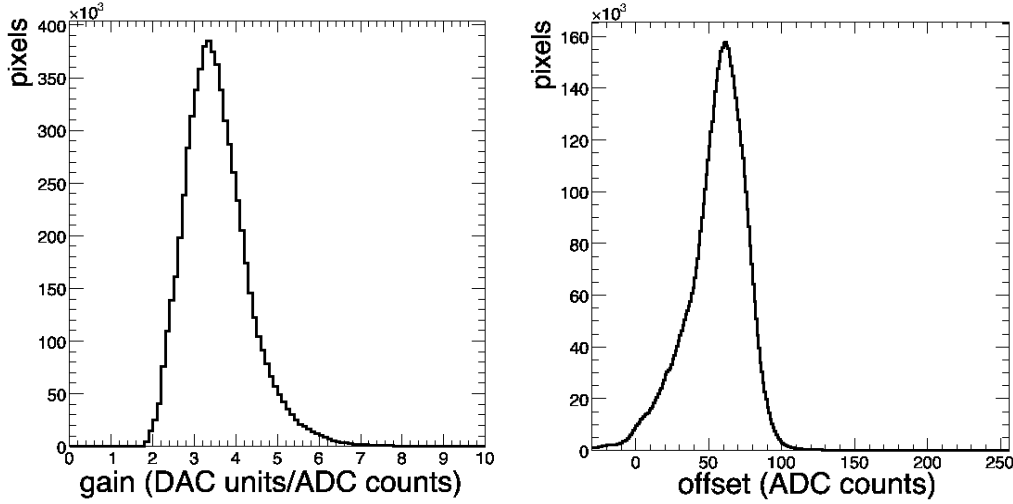


Figure 11. Slope (on the left) and offset (on the right) distributions extracted from the straight-line fits to the gain response curves of all pixels.

For high signals (above about 45000 electrons) the signal saturates in the pixel amplifier. Below that the response is approximately linear until at low charges the signal becomes non-linear again. The non-linearity on the high side does not hurt much and can be even beneficial to suppress the effect of delta-rays which deposit large amount of charge in a pixel and might spoil the position resolution. On the other hand the low charge non-linearity is more serious since it deteriorates the position resolution when interpolating between pixel charges. Attempt was made to optimize the ROC settings to minimize this non-linearity [10]. The distribution shown in figure 10 can be fitted by the formula:

$$ADC = p_3 + p_2 * \tanh(p_0 * VCAL - p_1), \quad (4.1)$$

which has 4 parameters. Parameter p_1 is related to the non-linearity in the lower charge region, the smaller it is the more linear the curve is. At p_1 equal to 1 the whole low energy region can be nicely fitted by a straight line. More details can be found in [10] where the p_1 parameter for BPIX before and after the optimization of the signal linearity is shown.

The 4-parameter formula 4.1 from above would be too complicated to use for 66 M pixels. For the hit position reconstruction a linear fit is used instead with 2 parameters: slope and offset. The measured distributions of both parameters are shown in figure 11.

The slope (gain) distribution has a mean at 3.6 and an RMS of about 0.5. The offset distribution has a mean at 55 ADC units (12700 electrons) and an RMS of 12.

4.6 Charge collection

During the cosmic-ray run at 3.8 T magnetic field the CMS tracker detected about 8.5 million tracks, from those about 77000 tracks were recorded in the pixel detector. These tracks are now being used to perform the initial detector alignment and to study the detector position resolution.

Using the calibration constants as presented in section 4.5 the charge distribution of pixel clusters can be measured. Figure 12 shows the cluster charge distribution normalized to $285\mu m$

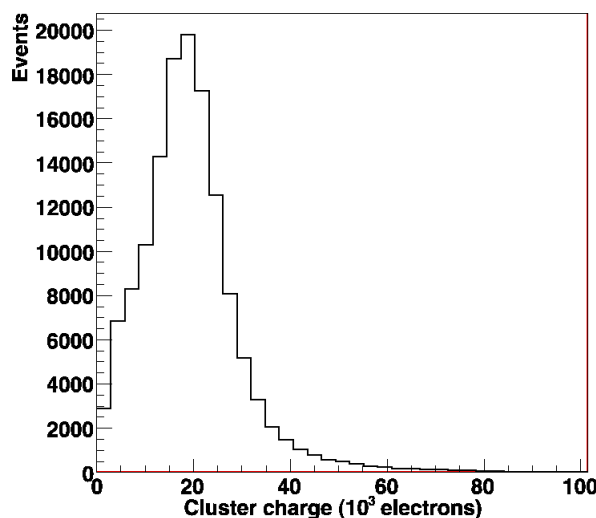


Figure 12. Cluster charge distribution in the barrel pixel detector normalized to a $285\mu\text{m}$ path in silicon

path, that is the total charge of each cluster is normalized to its path in silicon using the track angle information. The distribution shows the Landau like shape and peaks at about 21000 electrons as expected for full charge collection.

5 Conclusions

The CMS pixel detector has been successfully installed in CMS in July 2008. After two weeks of setup-time and testing the detector participated in a 3 month long series of CMS global runs including a cosmic-ray run with 3.8 T magnetic field. The pixel detector performed well, with only a few percent inefficiencies. The acquired data is been used for the detector alignment and performance studies. Next year, before the start of the LHC beam, more detailed calibrations will be performed in order to improve the detector operating parameters like e.g. lowering the thresholds.

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